REMARKS

Amendment to the claims

Claim 1 was amended to recite "*A circuit comprising:*

a camouflaged circuit structure having a gate region, including:

a substrate; a first active region of a first conductivity type being disposed in said substrate; a second active region of a first conductivity type being disposed in said substrate; and

a first well of said first conductivity type being disposed in said substrate under said gate region, said first well being in physical contact with said first active region and said second active region, wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit; wherein said first well is generally deeper than said first and second active regions;

the circuit further comprising a circuit structure having:

a second well of the first conductivity type being disposed in said substrate; and third and fourth active regions of a second conductivity type being disposed in said second well in contact with opposite sides of a gate region;

wherein said first well and said second well have a same depth and a same doping".

Support for reciting the circuit structure with the second well can for example be found in Figures 4a-c and the corresponding portion of the specification. In the example of Figures 4a-c, the transistor on the right of the figures comprises a second well 42 as recited in claim 1 as amended. As described in relation with Figures 4a-c the well 22 (first well in claim 1) and the well 42 (second well) are implanted in a same step with openings greater than or equal to the minimum n-well width (e.g. last line of page 11 of

the specification) and have both flat lower surfaces, whereby the two wells achieve same well characteristics, and share a same dopant, a same doping concentration, and a same depth.

Claim 6 was amended to recite: "*A semiconductor circuit comprising: a substrate having a first well of a first conductivity type; a first gate region being arranged above the first well; a plurality of first active regions of said first conductivity type disposed in said substrate, at least two of said plurality of first active regions being separated from one another by, and in physical contact with, said first well of said first conductivity type disposed in said substrate under said gate region; and a plurality of wells of a second conductivity type being partially disposed under said at least two of said plurality of active regions, wherein said plurality of wells of a second conductivity type are separated from said first well; the circuit further comprising:*

a second well of the first conductivity type;

a second gate region being arranged above the second well; and a plurality of second active regions of a second conductivity type disposed in said second well, at least two of said plurality of first active regions being separated from one another and in contact with opposite sides of the second gate region;

wherein said first well and said second well have a same depth and a same doping"

Support for reciting the circuit structure with the second well can for example be found in Figures 5a-d and the corresponding portion of the specification. In the example of Figures 5a-d, the transistor on the right of the figures comprises a second well 42 as recited in claim 6 as amended. As described in relation with Figures 5a-d the well 22 (first well in claim 6) and the well 42 (second well) are implanted in a same step and

have both flat lower surfaces, whereby the two wells achieve same well characteristics and share a same doping (same dopant, same doping concentration) and a same depth.

Dependent claims 2-5 and 14 were amended consistently with the new language of claim 1.

No new matter was added.

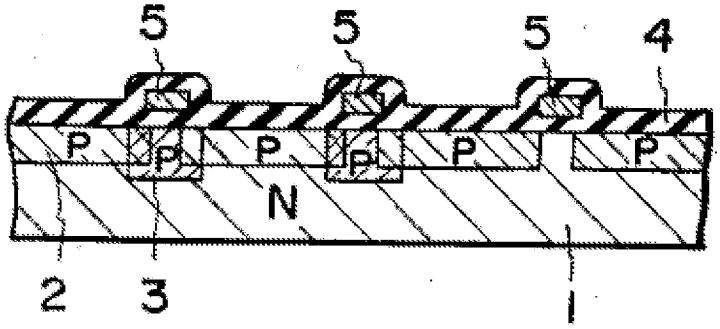
Rejections under 35 U.S.C. 102

Claims 1, 5 and 14 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,145,701 to Kawagoe. Applicants respectfully disagree.

Claim 1

Kawagoe teaches implementing a ROM with an array (see Fig. 4) of MIS FET transistors, wherein the transistors of each row of the array are connected in series and the gates of the transistors of each column are connected together. Information is stored in the ROM by implanting, or not, in the FET transistors deep channel layers (3) having a same type of conductivity as the active regions (see Fig. 6a, illustrated hereafter).

FIG.6a



Kawagoe teaches that a transistor with an implanted deep channel layer is a depletion transistor, wherein "*the MIS FET's of the depletion type are always in the 'on' state*" (col. 3, lines 26-27).

The Applicants note that the Examiner has failed to detail why Kawagoe's deep channel layer would read on a well that provides an electrical path "*regardless of any reasonable voltage applied to said circuit*". The Applicants note that Kawagoe's depletion MIS FETs are always 'on'. However, it is clear from Kawagoe that the depletion MIS FETs are always 'on' because their gate is never controlled to turn them 'off', and not because their deep channel layer would provides an electrical path "*regardless of any reasonable voltage applied to said circuit*".

Indeed, Kawagoe discloses (e.g. col. 3, lines 28-30) that "*the MIS FETs of the enhancement type can detect two levels of the 'on' state and the 'off' state*". Kawagoe further discloses (col. 3, lines 10-18) that the enhancement-type MIS FET's are such that "*at a gate voltage of zero V, no channel is formed and the connection between the source and drain is in the cutoff state, and when a certain threshold voltage is applied to the gate electrode, the channel is formed for the first time and the connection between the source and drain falls into the conductive state*". It follows that a positive or null gate-source voltage is applied to the gates of the enhancement-type MIS FETs of Kawagoe.

Further, the gates of the enhancement-type MIS FETs and depletion-type MIS FETs of Kawagoe are connected together. It follows that only a positive or null gate-source voltage is applied to the gates of the depletion-type MIS FETs of Kawagoe. The skilled person knows well that one needs to apply a negative gate-source voltage to turn "off" a depletion-type FET. Kawagoe's depletion-type MIS FETs are therefore always "on" because they are arranged in a circuit that does not provide their gates with a voltage adapted to turn them "off", and not because their deep channel layers would have a structure such that they provide an electrical path "*regardless of any*

reasonable voltage applied to said circuit". At least in view of the above, the Applicants respectfully submit that the deep channel layer of Kawagoe relates to a structure that differs completely from the well recited in claim 1 as pending.

This being said, and in order to move the application to issue, the Applicants have amended claim 1 to recite, in addition to the structure already recited in claim 1, "*a circuit structure having:*

a second well of the first conductivity type being disposed in said substrate; and third and fourth active regions of a second conductivity type being disposed in said second well in contact with opposite sides of a gate region;

wherein said first well and said second well have a same depth and a same doping".

The Applicants respectfully submit that the Examiner has failed to show that Kawagoe would disclose or even suggest a circuit as recited in claim 1, and in particular comprising: "*a circuit structure having:*

a second well of the first conductivity type being disposed in said substrate; and third and fourth active regions of a second conductivity type being disposed in said second well in contact with opposite sides of a gate region;

wherein said first well and said second well have a same depth and a same doping".

The Applicants respectfully submit that at least in view of the above difference, claim 1 as amended is not anticipated by, nor obvious over, Kawagoe, and is therefore patentable in view of Kawagoe.

Claims 5 and 14

Claims 5 and 14 depend on claim 1. Applicants respectfully submit that at least in view of their dependency on claim 1, claims 5 and 14 are patentable over Kawagoe.

Rejections under 35 U.S.C. 103

Claims 2, 3 and 4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kawagoe in view of U.S. Pat. No. 3,938,620 to Spadea; and Claim 6 stands rejected as being unpatentable over U.S. Pat. No. 6,740,942 to Baukus ('942) in view of U.S. Pat. No. 5,973,375 to Baukus ('375). The Applicants respectfully disagree.

Claims 2, 3 and 4

Claims 2, 3 and 4 depend directly or indirectly on claim 1. Applicants note that the Examiner has failed to show that Spadea shows a circuit as recited in claim 1, and in particular comprising: "*a circuit structure having:*

a second well of the first conductivity type being disposed in said substrate; and third and fourth active regions of a second conductivity type being disposed in said second well in contact with opposite sides of a gate region;

wherein said first well and said second well have a same depth and a same doping".

At least in view of the above, Applicants submit that the Examiner has failed to show that Kawagoe or Spadea, alone or in combination, would have led one of ordinary skill to a structure as recited in claim 1, and in particular "*wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit*". Accordingly, Applicants respectfully submit that claim 1 is patentable over Kawagoe in view of Spadea, and respectfully submit that at least in view of their dependency on claim 1, claims 2, 3 and 4 are patentable over Kawagoe in view of Spadea.

Claim 6

The Applicants note that the Examiner has failed to show that either '942 or '375, alone or in combination, would disclose or suggest "*a second well of the first conductivity type;*

a second gate region being arranged above the second well; and a plurality of second active regions of a second conductivity type disposed in said second well, at least two of said plurality of first active regions being separated from one another and in contact with opposite sides of the second gate region;

wherein said first well and said second well have a same depth and a same doping" as recited in claim 6 as amended.

At least in view of the above difference, the Applicants respectfully submit that the Examiner has failed to show that any combination of '942 and '375 would have led one skilled in the art to a circuit as recited in claim 6 as amended, whereby claim 6 as amended is patentable over '942 and '375.

* * *

In view of the above, Applicants submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

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